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| 10/579,383 | 05/11/2006 | Milind M. Kulkarni | NL03 1316 US1 | 8189 |

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PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
INTELLECTUAL PROPERTY & STANDARDS
370 W. TRIMBLE ROAD MS 91/MG
SAN JOSE, CA 95131

| EXAMINER | |
|---|---|
| MYERS, PAUL R | |
| **ART UNIT** | **PAPER NUMBER** |
| 2111 | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/579,383 | KULKARNI ET AL. | |
| | Examiner | Art Unit | |
| | Paul R. Myers | 2111 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 13* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/11/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to because the rectangular box(es) shown in the drawings should be provided with descriptive text labels. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In regards to claim 5: Claim 5 has two appearances of the word "position". With each having a different definition. One being the order in a sequence and the other being a physical location in space. In reviewing applicants specification the examiner concludes the claim is to read that the sequential position of the address corresponds to the physical position of the data words are placed on the data lines. The examiner had given a 112 1st before realizing that two different definitions of position was being used.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 6-7, 9-11, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable in view of Dill et al PN 4,667,305 and Tran et al PN 5,901,294.

In regards to claims 1, 9, 13: Dill et al teaches an electronic data processing circuit , the circuit comprising: a plurality of data handling units (processors, storage units, buffers, display terminals, input/output devices and the like Column 1 lines 15-22) with data outputs (such as from the processors and the storage units), at least part of the data handling units (such as the processors) having address outputs (address); a bus (bus abstract) with address lines (address)

and data lines (data bus), the data lines supporting simultaneous transfer of up to a maximum number of bits in a bus cycle ($N_c$); a bus control to control access to the bus in successive access cycles (if $N_f$ extends past the end of the bus width then the bus bits "wrap around" and the address is incremented for the next cycle), the bus control being arranged to cause data bits from a plurality of data words of less than said maximum number of bits ($N_c$) from respective ones of the data handling units (processors and the storage units), to be placed in combination on the data lines in a same bus cycle (processors and the storage units), the bus control causing write addresses that the respective ones of the data handling units (processors and the storage units ) supply for respective ones of the plurality of data words to be placed on the address lines in a plurality of respective bus cycles (with wrap around).

Dill et al's system is a distributed system and does not expressly teach a separate controller.

Tran et al teaches an electronic data processing circuit (Figure 1), the circuit comprising: a plurality of data handling units (12-18) with data outputs (AD0-AD1), at least part of the data handling units (12-16) having address outputs (AD0-AD1); a bus (22) with address lines (AD0-AD1) and data lines (AD0-AD1), the data lines supporting simultaneous transfer of up to a maximum number of bits in a bus cycle (256); a bus controller (20) coupled to the data handling units (12-18) and arranged to control access to the bus in successive access cycles (via grant lines), the bus controller being arranged to cause data bits from a plurality of data words of less than said maximum number of bits (64 bits, 128 bits or 192 bits) from respective ones of the data handling units (12-18), to be placed in combination on the data lines in a same bus cycle (simultaneous Abstract), the bus controller causing write addresses that the respective ones of the

data handling units (12-18) supply for respective ones of the plurality of data words to be placed on the address lines.

Tran et al does not teach the address handling when in a plurality of respective bus cycles.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to either include the wrap around feature of Dill et al in the system of Tran et al or to include a centralized controller such as described by Tran et al in the system of Dill et al. All the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

In regards to claims 2, 10-11: both Dill et al and Tran et al teach the data handling units support a variable word size, and adapting a number of words in the plurality of data words that is placed on the data lines to the word size or word sizes supplied by the data handling units.

In regards to claim 6: Both Dill et al and Tran et al teach one of the data handling units being a memory and reading from the memory.

In regards to claim 7: Dill et al teaches adding an address cycle if there is wrap around.

6. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dill et al PN 4,677,305 and Tran et al PN 5,901,294 as applied to claim 1 above, and further in view of "Reordering Memory Bus Transactions for Reduced Power Consumption" herein after Childers et al.

In regards to claims 3-4: Both Dill et an and Tran et al teach deciding where on the bus to place the data. Neither however teaches deciding where to place the data on the bus being based upon minimizing the Hamming Distance. Childers teaches selecting the order in which data is placed on the bus to minimize the Hamming distance. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use the Hamming distance to select the where the data from the plurality of data handling units is placed on the bus because this would have reduced power consumption.

In regards to claim 5: Tran et al teaches 4 separate positions for data and 4 separate address each 64 bits corresponding to the data bit positions. The examiner notes Tran et al has 4 addresses presented in a single address cycle which both sequentially and physically correspond with the 4 bit positions of the 4 data cycles. The examiner was unable to find multiple sequential address cycles corresponding to the bit positions of the bits in a single data cycle.

7. Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Dill et al PN 4,677,305 and Tran et al PN 5,901,294 as applied to claim 1 above, and further in view of Dornier et al PN 5,561,772.

In regards to claim 8: Neither Dill et al nor Tran et al expressly teach burst transactions. Dornier et al teaches a burst mode (Figure 6). It would have been obvious to a person of ordinary skill in the art at the time of the invention to include burst transfers because this would have removed unnecessary address cycles.

### *Allowable Subject Matter*

8. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The examiner notes the correspondence and difference between claims 12 and 5.

### *Conclusion*

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 571 272 3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul R. Myers
Primary Examiner
Art Unit 2111

/Paul R. Myers/
Primary Examiner, Art Unit 2111